A Symmetric Wideband Doherty Power Amplifier for the n78 - 5G NR Frequency Band

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***Abstract*—This paper describes the design of a wideband Doherty power amplifier for fifth generation mobile network applications in sub-6 GHz frequency bands. The presented symmetric design uses different drain-supply voltages for the main and peaking amplifiers to achieve high efficiency at deep power back-off levels. The advantages and disadvantages over conventional asymmetric designs are discussed focusing on the case of wideband Doherty power amplifiers. A new Doherty combiner is proposed which equalises the impedance transformation ratio between the back-off and peak power points. Finally, a proof-of-concept prototype is developed which can achieve higher than 50% drain efficiency for power levels between peak output power and 8 dB power back-off, for the frequency range between 3.3 GHz and 3.8 GHz.**

***Index Terms*—Doherty, energy efficiency, high-PAPR, power amplifier, wideband, GaN-HEMT.**

I. Introduction

With emerging cellular network technologies, large quantities of spectrum at higher frequency bands are being allocated to support the new requirements for high data rates. In the new base stations, the energy efficiency of the transmitters might become an important limitation due to thermal management. Since the power amplifier is usually the most significant contributor to the total power consumption and heat dissipation of the transmitter, difficult targets must be met for its minimum permissible efficiency. In addition, due to the high peak-to-average power ratio PAPR of the transmitted signals, special efficiency-enhancement techniques are required to increase the efficiency of the power amplifier not only at peak power, but also at deep power back-off levels.

Among several possible efficiency-enhancement techniques, the Doherty load modulation technique has been extensively studied. It is also the most ubiquitously used technique owing to its simplicity, which allows integration of the Doherty architecture into power amplifier modules with relatively low cost and small footprint. Therefore, such power amplifier modules are ideal candidates for future highly efficient massive-MIMO base stations, which would require many such modules to drive the multiple antenna elements.

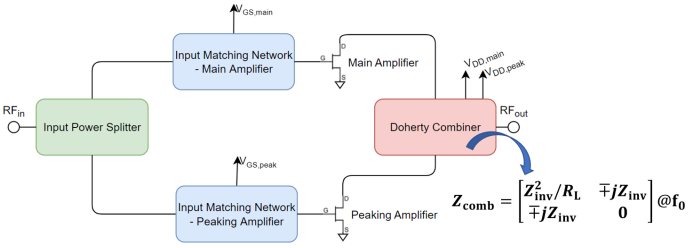

Fig. 1. Block diagram of typical Doherty PA topology targeted for cellular network applications. Bottom right is the impedance matrix of the Doherty combiner in the general case, when studied as a 2-port network as shown in [1], with Port 1 towards the Main PA and Port 2 towards the Peaking PA. Z_{inv} indicates the characteristic impedance of the $\lambda/4$ impedance inverter and R_{L} is the impedance of the RF load. The sign of the terms $Z_{1,2}$ and $Z_{2,1}$ depends on the exact combiner topology.

Although it is clear that the Doherty technique can greatly increase the average efficiency for limited RF bandwidths, significant research effort has been concentrated on new Doherty-like topologies which can cover the wide bandwidths required for future cellular networks. Even at the Doherty topology of Fig.1, certain parameters can be tuned to extend the bandwidth of the original topology. Important examples of such bandwidth extension are described in [1] and [2].

This paper investigates the use of different drain supply voltages for the main and peaking amplifiers to achieve deep output power back-off $OPBO$, instead of using asymmetric device sizes which is the conventional approach. In [3] the possibility of using either device asymmetry or unequal drain supply voltages to achieve deep $OPBO$ is discussed. Additionally, with different drain supply voltages it is possible to use the same device size for both the main and peaking amplifiers, which in turn implies several other advantages, especially for wideband designs. A main target of this work is to show these advantages and develop relationships to

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calculate related performance trade-offs. Finally, a proof-of-concept symmetric Doherty PA demonstrator is developed with unequal drain supply voltages using a standard 28 V GaN-HEMT technology. The demonstrator achieves high efficiency at the 8 dB $OPBO$ level and can cover the n78 5G-NR frequency band (3.3 GHz - 3.8 GHz).

II. Design Equations & Trade-offs

A. Generalized Doherty Combiner Design Equations

A generalized theoretical analysis for the 6 dB $OPBO$ case has already been developed in [2]. Here, some design equations are further generalized for any $OPBO$ level in Table I. Since the impedance transformation ratio ITR has been closely linked to the usable bandwidth of the Doherty combiner, it is used in Table I as a design parameter and all other parameters are calculated through the chosen ITR. Furthermore, it is assumed that both the main & peaking devices are from the same technology, such that there exists a nominal drain supply voltage $V_{\text{DD,nom}}$ which would be close to the maximum permissible drain supply voltage for device reliability. For the equations in Table I it is assumed that the drain supply voltages of the main & peaking devices should not exceed this $V_{\text{DD,nom}}$.

The knee voltage V_{knee} can be chosen for initial calculations as 10% of $V_{\text{DD,nom}}$. Some additional useful relationships for the design of the Doherty combiner can be:

$$\begin{aligned} R_{\text{opt,main,pp}} &= 2(V_{\text{DD,main}} - V_{\text{knee}})/I_{\text{max,main}} \\ &= R_{\text{opt,main,nom}} \frac{V_{\text{DD,main}} - V_{\text{knee}}}{V_{\text{DD,peak}} - V_{\text{knee}}} \end{aligned} \tag{1}$$

$$\begin{aligned} R_{\text{opt,peak,pp}} &= 2(V_{\text{DD,peak}} - V_{\text{knee}})/I_{\text{max,peak}} \\ &= R_{\text{opt,main,nom}}/DSR \end{aligned} \tag{2}$$

$$R_{\text{opt,main,bo}} = 2\frac{V_{\text{DD,main}} - V_{\text{knee}}}{I_{\text{main}}(x_b)} = \frac{R_{\text{opt,main,pp}}}{x_{\text{b}}} \tag{3}$$

which are respectively, the optimum load impedance for the main amplifier at peak power, the optimum load impedance for the peaking amplifier at peak power and the optimum load impedance for the main amplifier at the back-off point.

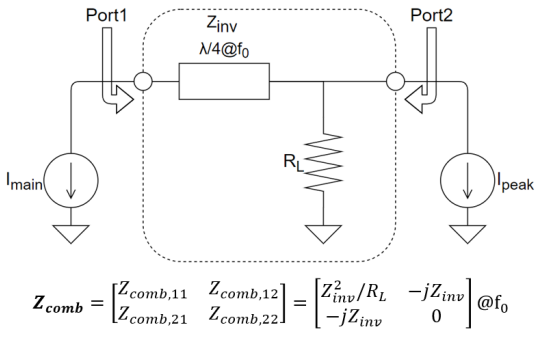


Fig. 2. Simplified schematic of Doherty combiner used for analysis purposes. The impedance matrix for this simplified case is shown. With the design equations from Table I the impedances of the combiner elements and the supply voltages are calculated to maximize efficiency in the back-off point and at peak power.

TABLE I
Generalized Design Equations

Parameter	*Description*	*Calculation*
x_{b}	back-off point	$10^{-OPBO/20}$
ITR	impedance transformation ratio	usually chosen[a] between $[x_{\text{b}}^2, 1]$
DSR	device size ratio ($I_{\text{max,peak}}/I_{\text{max,main}}$)	$\frac{1-x_b}{\sqrt{ITR}}$
$V_{\text{DD,main}}$	drain supply voltage of the main amplifier	$\frac{(V_{\text{DD,nom}}-V_{\text{knee}})}{\sqrt{ITR}}x_{\text{b}}+$ $+V_{\text{knee}}$
$V_{\text{DD,peak}}$	drain supply voltage of the peaking amplifier	$V_{\text{DD,nom}}$
R_{L}	RF load impedance[b]	$R_{\text{opt,main,nom}}\sqrt{ITR}$
Z_{inv}	characteristic impedance of $\lambda/4$ impedance inverter[b]	$R_{\text{opt,main,nom}}$
I_{main}	main current function	$x \cdot I_{\text{max,main}}/2$
I_{peak}	peaking current function[c]	$k(x)\frac{I_{\text{max,main}}}{2}e^{-j\theta}$

[a] the ITR is defined as $ITR = R_{\text{L}}/R_{\text{opt,main,bo}}$
e.g. in the conventional Doherty $x_{\text{b}} = 0.5$ and $ITR = x_{\text{b}}^2 = 1:4$

[b] $R_{\text{opt,main,nom}} = 2(V_{\text{DD,nom}} - V_{\text{knee}})/I_{\text{max,main}}$

[c] $k(x) = \begin{cases} 0 & ,0 \le x < x_{\text{b}} \\ (\text{x-x}_{\text{b}})/\sqrt{ITR} & ,x_{\text{b}} \le x \le 1 \end{cases}$

[d] The variable x is a normalized voltage signifying the level of the input signal

B. Relationships for performance trade-offs

The relationship (4) outlines a design space for the Doherty combiner. For a specific back-off point x_{b} either the drain supply voltage ratio or the device size ratio DSR can be used, to achieve a range of Doherty combiner designs with different performance. On the one extreme the same supply voltage can be used for both main & peaking devices, thus $ITR = {x_{\text{b}}}^2$ which is the conventional case. On the other extreme $Z_{\text{inv}} = R_{\text{L}}$ can be chosen, thus $ITR = 1$ as shown in [1]. Then the design space is $ITR \in [{x_{\text{b}}}^2, 1]$. In this subsection important performance parameters will be linked to this impedance transformation ratio.

$$DSR\frac{V_{\text{DD,peak}} - V_{\text{knee}}}{V_{\text{DD,main}} - V_{\text{knee}}} = \frac{1 - x_{\text{b}}}{x_{\text{b}}} \tag{4}$$

1) Calculating the power utilization factor (PUF): If the drain supply voltage ratio from (4) is used to achieve a back-off point, the main supply-voltage is lowered below the nominal (the peaking-supply voltage remains equal to the nominal $V_{\text{DD,nom}}$, which is also the maximum allowed as

previously discussed). This means that the saturated RF output power of the main PA ($P_{\text{sat,main}}$) will be lower than the nominal saturated output power($P_{\text{sat,main,nom}}$). This decrease in the total saturated output power can be expressed using the power utilization factor:

$$\begin{aligned} PUF = & \frac{P_{\text{sat,main}}+P_{\text{sat,peak}}}{P_{\text{sat,main,nom}}+P_{\text{sat,peak,nom}}} \\ = & (x_{\text{b}}\frac{V_{\text{DD,peak}}-V_{\text{knee}}}{V_{\text{DD,main}}-V_{\text{knee}}}+1-x_{\text{b}})^{-1} \end{aligned} \quad (5)$$

2) Gain reduction due to reduction of the main drain supply voltage: Depending on the device technology used and the frequency band of the application the power transistors might offer limited gain. At higher frequency bands the gain roll-off of the power transistors starts becoming an important consideration. On top of that, due to the input power splitter, the gain of the Doherty PA experiences an additional gain reduction of at least 3 dB nominally (even more for uneven splitting). Finally, due to the difficulty of achieving wideband input matching conditions with large power transistors, an additional impact on the gain should be expected.

With all these factors accumulating, the maximum available gain (G_{MAX}) should be conserved as much as possible. On the other hand, lowering the main supply voltage $V_{\text{DD,main}}$ in order to achieve a deep back-off point, will unavoidably lead to reduction of G_{MAX} due to increase of the parasitic capacitances of the transistors, which are voltage dependent. With further decrease of the gain due to lowering of the main supply voltage it might be difficult to meet design targets. Thus an important design trade-off can be derived between the supply voltage ratio and G_{MAX}, although an analytical expression cannot be reached since the relationship is largely technology dependent.

3) Estimation of the usable bandwidth: As discussed in [1], [2] the impedance transformation ratio ITR can be used to calculate the bandwidth limitation of the Doherty combiner. In fact, the ITR is more related to operation at the back-off point where the $\lambda/4$ impedance inverter of the Doherty combiner transforms the load impedance R_{L} into the targeted load impedance $R_{\text{opt,main,bo}}$ for the main amplifier. However, it is important to also consider the operation at peak power to have a more complete picture for the usable bandwidth of the Doherty combiner.

An improved estimation method is shown in [4], by calculating the effective loads of the main & peaking PA's from (6) and (7). Then, a load reflection coefficient can be calculated using as reference impedance, the targeted impedance at peak power and at back-off, from (1)-(3). Finally the bandwidth can be calculated from the frequencies for which the load reflection coefficients would stay within a p-dB compression output-power contour, which in turn can be calculated from loadpull theory.

$$Z_{\text{load,main}} = Z_{\text{comb,11}} + Z_{\text{comb,12}}\frac{I_{\text{peak}}}{I_{\text{main}}} \quad (6)$$

$$Z_{\text{load,peak}} = Z_{\text{comb,22}} + Z_{\text{comb,21}}\frac{I_{\text{main}}}{I_{\text{peak}}} \quad (7)$$

For the bandwidth estimation to be valid, all components causing frequency dependency should be included as part of the Doherty combiner, even estimations for the device parasitic capacitances and packaging parasitics. In addition, due to the term $e^{-j\theta}$ in the peaking current, the input power splitter which determines the phase θ will also introduce some frequency dependency which should be taken into account. For example, an ideal quadrature hybrid splitter might be modelled with a constant $\theta = 90°$, or a wilkinson splitter plus $\lambda/4$ line might be modelled as $\theta = 90° \frac{f}{f_0}$. Finally, in many cases it is also possible to calculate an optimum $\theta = \theta(f)$, such that the voltage swing of the main & peaking amplifiers is maximized without zero-crossing of the drain voltage waveforms in the entire bandwidth of interest, in which case the efficiency would also be maximized.

4) Choosing main & peaking device sizes and the special case of $DSR = 1$: Although any DSR from Table I is possible, in the special case $DSR = 1$ the main & peaking devices can be identical, which might imply some advantages. Firstly, it is rarely possible to implement any arbitrarily chosen DSR, since RF power transistors are usually available in a very limited number of sizes. It is still possible to design for a deep back-off point by simply adjusting the drain supply voltages and the Doherty combiner, as shown in Table I. In fact, for wideband Doherty combiner designs, having a large peaking device, implies much larger drain parasitic capacitance compared to the main device, which can also be much more difficult to compensate due to its size. Thus it would be beneficial to keep a DSR close to 1, while a high DSR can "push" the design towards more narrowband combiner topologies.

When choosing the device sizes it might also be important to consider limitations caused by the input matching networks. The input matching networks can introduce additional frequency dependency in θ which can have a negative effect in the wideband behavior of the Doherty combiner. Another issue is the input impedance of the peaking amplifier which in the Doherty PA of Fig.1 would be biased in Class C. The input impedance of a Class C amplifier is not only frequency dependent but also significantly input-power as well as load dependent, complicating the design of the input matching network. Furthermore, since the input reflection of asymmetric main & peaking amplifiers is not the same, the isolation of the input power splitter would be compromised and the two branches can interact at their input side, further complicating the design. The previous issues can be avoided when $DSR = 1$, since by using the same device size for the main and peaking PA's, it is also possible to use nearly the same input matching network for both branches. Then the frequency dependencies of the two branches would subtract each other and their effect on θ is largely eliminated. Moreover, the input reflections of the two branches are closely matched and the isolation of the input power splitter can be better utilized. The tuning of

the input matching networks during prototyping would also be simplified, since a change in the input matching of one branch would need to simply be mirrored on the other branch. Overall, the multiple benefits of the special case $DSR = 1$ can accumulate to boost the bandwidth of the Doherty PA of Fig.1.

III. Design of a Wideband Doherty PA

In this design example the goal was to design a Doherty PA with $8\ dB\ OPBO$ using a standard $28\ V$ GaN-HEMT technology, for the n78 5G-NR band (3.3-3.8 GHz). The topology used to implement the combiner in this example was a type of inverted-Doherty as shown in Fig.3. An important addition in this topology is the $\lambda/2$ extension line between the peaking PA and the RF load, for which it was chosen $Z_{\text{ex}} = R_{\text{opt,peak,nom}}$. The drain parasitic capacitances $C_{\text{DS,main}}$ & $C_{\text{DS,peak}}$ are resonated at the center frequency with the shunt inductances $L_{\text{d,main}}$ & $L_{\text{d,peak}}$.

A. Equalisation of the impedance transformation ratio

As mentioned previously, the parameter ITR can be used to estimate the usable bandwidth of the Doherty combiner in the back-off, however it is important to also consider the operation at peak power. Thus a similar impedance transformation ratio can be defined for peak power.

$$ITR_{\text{pp}} = \frac{R_{\text{opt,main,pp}}}{R_{\text{L,mod}}} = \frac{x_{\text{b}}^2}{ITR} \tag{8}$$

In (8), $R_{\text{L,mod}}$ is the effective load impedance at the node of the RF load R_{L}, due to load modulation. By equating $ITR_{\text{pp}} = ITR$, the impedance transformation ratio will be maximized both in the back-off point and at peak power, such that a best trade-off case is derived $ITR = x_{\text{b}}$. Additionally, for an $8\ dB\ OPBO$ an $ITR = 0.3981$ and $DSR = 0.9539$ is calculated, meaning that it is possible to use identical devices for the main & peaking amplifiers and the benefits of the special case $DSR = 1$ can be utilized.

B. Usable bandwidth estimation

The simplified circuit in Fig.3 was used to study the relationship between the ITR and the usable bandwidth of the Doherty combiner. To model the parasitic drain capacitances, it was calculated $(2\pi f_0 C_{\text{DS,main}})^{-1} = R_{\text{opt,main,nom}}$ & $(2\pi f_0 C_{\text{DS,peak}})^{-1} = R_{\text{opt,peak,nom}}$ at $f_0 = 3.55\ GHz$, since it seems from loadpull data of GaN-HEMT devices in the n78 frequency band, that the reactances of these capacitances are close to the optimal load impedance of the devices. The component values were calculated for the same saturated output power target and $OPBO = 8\ dB$. The relationship between the estimated usable bandwidth and the ITR was estimated using the previously discussed evaluation method and $p = 1\ dB$ and is shown in Fig.4. To show how the choice of the input power splitter can affect the usable bandwidth, three cases are shown. The first & second are conventional splitters often used in the topology of Fig. 1, while the final case is an approximation of the calculated "optimal" $\theta = \theta(f)$ and can maximize the usable bandwidth for most ITR's. An important conclusion from these graphs is that higher ITR does not necessarily create a larger usable bandwidth, which has been the conclusion in previous works. The calculated equalised $ITR = x_{\text{b}}$ should provide a universal "best trade-off" case.

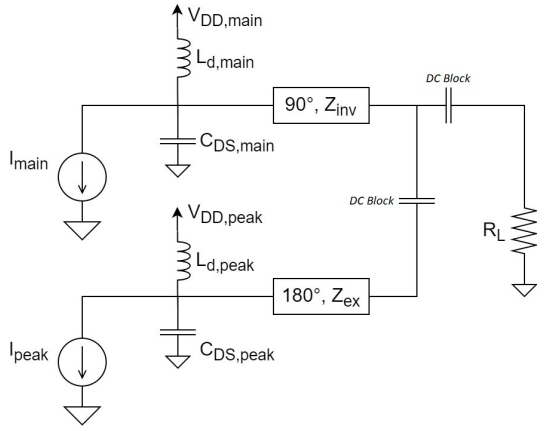


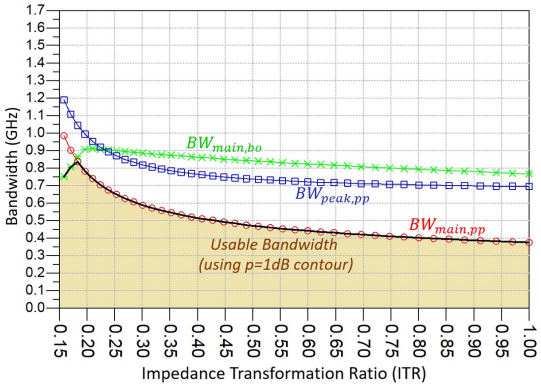
Fig. 3. Simplified schematic circuit showing the basic topology of the designed Doherty combiner. An extension line was added between the peaking PA and the RF load. This simplified circuit was used to investigate the relationship between the ITR and the usable bandwidth of the Doherty combiner.

C. Doherty Combiner Design

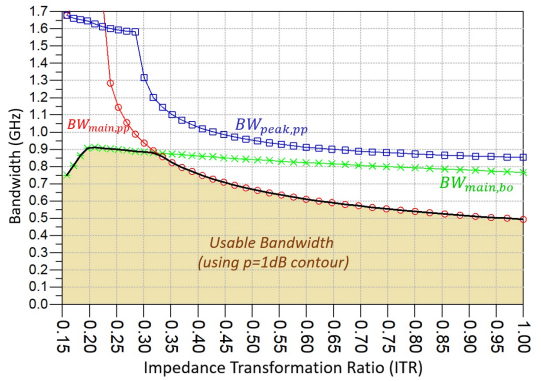
To simplify the demonstrator design, a standard SMD component quadrature hybrid was used for the input power splitter. Then, the usable bandwidth estimation from Fig.4 is approximately 500 MHz for the Doherty combiner, which is sufficient for the application. For the used technology $V_{\text{DD,nom}} = 28\ V$, thus $V_{\text{DD,main}} = 18.7\ V$. Finally $PUF = 81.1\%$ meaning that a $0.91\ dB$ reduction from the combined rated output power of the devices should be expected. For the transistor dies used in this prototype, it was calculated based on simulated loadpull data that $R_{\text{opt,main,nom}} = 18.6\ \Omega$, thus $R_{\text{L}} = 11.73\ \Omega$, $Z_{\text{inv}} = 18.6\ \Omega$ and $Z_{\text{ex}} = R_{\text{opt,peak,pp}} = 19.5\ \Omega$. The $50\ \Omega$ RF load impedance was converted to the targeted R_{L} value using a two-step impedance transformer. After optimization and EM simulation of the Doherty combiner PCB, the achieved load contours can be seen in Fig.5 and are comparable to the targeted load contours calculated from the simplified circuit of Fig.3, owing to the relatively small bondwire inductance.

D. Input Matching Network Design

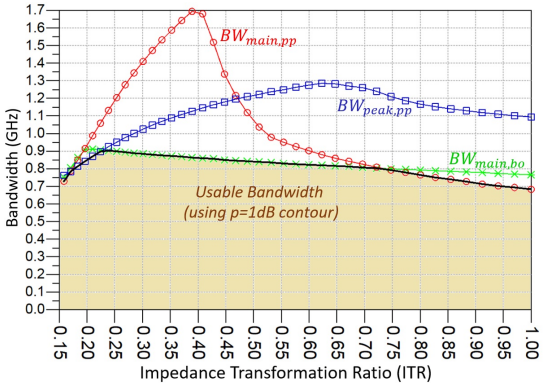
High power RF transistors have relatively low input impedance making wideband input matching with high return loss somewhat challenging. Instead, high return loss is achieved only for the higher frequencies and the lower frequencies are intentionally mismatched to flatten the gain inside the frequency band of interest. As discussed previously, the input matching networks for both branches are virtually identical. This fact accelerated significantly the design, as well as the tuning of the prototype.



a) Quad. hybrid splitter, phase delay $\theta_1(f) = 90°$



b) Wilkinson splitter + $\lambda/4$ transmission line, phase delay $\theta_2(f) = 90° \frac{f}{f_0}$



c) Quad. hybrid splitter + $\lambda/2$ transmission line, phase delay $\theta_3(f) = 90° - 180° \frac{f}{f_0}$

Fig. 4. Estimated usable bandwidth around the center frequency for a range of Doherty combiners of the type shown in Fig.3. Each graph shows the estimation using a different type of phase delay. All of the Doherty combiners tested are designed for the same peak power and $OPBO$ but each one achieves a different impedance transformation ratio (ITR). The green, red & blue bandwidth limitations are respectively caused by the main PA at back-off, the main PA at peak power & the peaking PA at peak power. The green limitation is the same in all three graphs because the choice of $\theta(f)$ does not affect the operation at the back-off point.

E. Prototyping Method

A Doherty PA prototype was designed based on a bare-die approach. Two identical GaN-HEMT devices, each rated

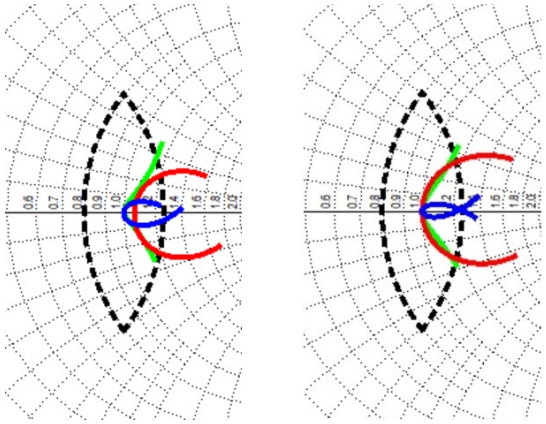


Fig. 5. Left: load contours of the optimized em-simulated combiner. Right: targeted load contours, which were calculated using the topology of Fig.3. The usable bandwidth of the combiner is calculated from the frequencies for which the load contours stay inside the $p = 1\ dB$ compression contour (dashed). The above load contours were calculated assuming a quadrature hybrid input power splitter. The green, red & blue contours are respectively the load reflection coefficients "seen" by the main PA at back-off, the main PA at peak power & the peaking PA at peak power.

for $44.5\ dBm$ saturated output power were used for the main & peaking amplifiers. The bare transistor dies were silver-sintered directly on a copper-carrier heatsink which had been nickel-gold plated.

The PCB's of the Doherty combiner, input matching networks and power splitter were designed using 10mil RO4350B material. It was possible to manually align on the copper-carrier the PCB's very close to the transistor dies. Finally the transistor dies were bonded directly to the PCB's using very short bonding wires. The bonding wire array inductance had been extracted from previous experiments with this method and is minimal, on the order of $110\ pH$.

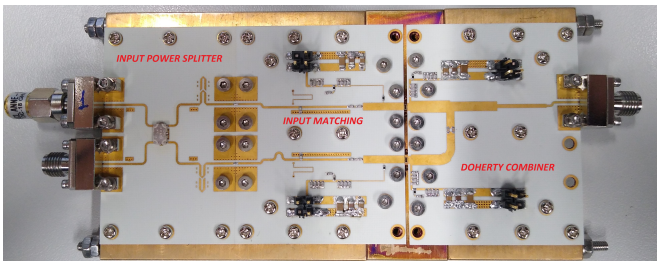


Fig. 6. Assembled Doherty PA prototype. Bare GaN dies are used resulting in short bonding wires with very low parasitic inductance. Due to this low inductance it was possible to ignore the bond wires in previous analysis, although some optimization is needed on the width & length of the impedance-inverter & extension line, in order to achieve the designed characteristic impedances and electrical lengths. The inductances $L_{\text{d,main}}$, $L_{\text{d,peak}}$ are implemented using the drain-supply stubs. A 2-step impedance transformer is used to transform the 50 Ω load impedance into the designed R_{L}.

F. Measured Performance

The performance of the Doherty PA prototype was evaluated using power sweep of a pulsed RF signal, with a pulse period of 200 μs and a pulse width of 20 μs. The measurement of

the input and output RF power was performed using calibrated wideband power sensors, while the measurement of the DC current consumption was performed using current clamps. The measurement of the RF power & DC power consumption was performed only in the last 10 μs of the RF pulse to allow the pulse ripple to settle. The measured performance of the prototype was sufficiently close to the performance expected from simulation, although it was not possible to drive the prototype into sufficient saturation to estimate the maximum output power, due to source power limitation of the measurement setup.

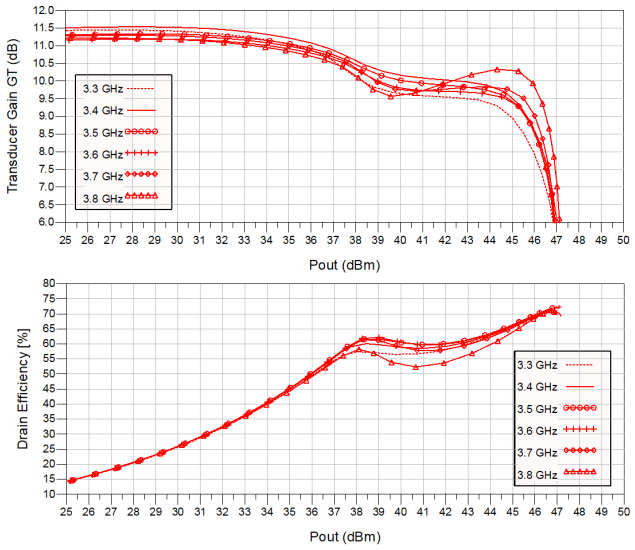


Fig. 7. Simulated performance of the assembled Doherty PA prototype. The different sweeps are for the frequencies from 3.3 GHz to 3.8 GHz with step of 0.1 GHz

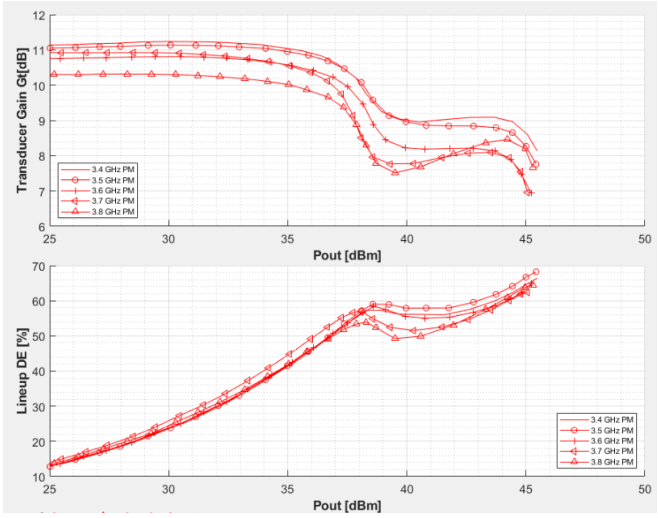


Fig. 8. Measured performance of the assembled Doherty PA prototype. Due to source power limitation of the measurement setup, it was not possible to drive the prototype into sufficient saturation to show the achievable saturated output power. Nevertheless, the measured performance is sufficiently close to the simulated.

IV. Conclusion

A symmetric Doherty power amplifier was designed which achieves high efficiency at 8 dB $OPBO$ and can cover the 3.3 GHz to 3.8 GHz frequency band. The design prooves that symmetric Doherty designs can achieve high efficiency and deep power back-off levels but with many advantages in the case of $DSR = 1$, compared to asymmetric designs, especially for operation over wide frequency bandwidths. It was shown that increasing the ITR might not always be beneficial for the usable bandwidth of the Doherty combiner. Finally, a special Doherty combiner design was presented with equalised ITR which should achieve a universal best trade-off for most combiner topologies.

Acknowledgment

This project has received funding from the ECSEL Joint Undertaking (JU) project UltimateGaN under grant agreement No 826392. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Austria, Belgium, Germany, Italy, Slovakia, Spain, Sweden, Norway, Switzerland.

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